Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1 (currently amended). A data processing system, comprising:

~~[at least one main processor]~~ multiple main processors connected to a system bus;

a system memory connected to the system bus and accessible to ~~[each of]~~ the main processors;

error ~~[logic configured]~~ logic, external to the main processors, and configured to receive internal error signals asserted by ~~[one or more of]~~ the main processors and to respond to an internal error signal by disabling ~~[the]~~ a main processor asserting ~~[the]~~ an internal error signal and restarting the system with any remaining functional ~~[processors]~~ main processors, wherein the error logic includes an error status register accessible via an I2C bus; and

a service processor configured to receive a service processor interrupt generated by the error logic.

2 (original). The system of claim 1, wherein the error logic is further configured to record the internal error signal in an error status register of the error logic.

3 (original). The system of claim 2, wherein the error status register includes at least a pair of bits corresponding to each of the main processors, wherein a first bit of each pair is indicative of whether the corresponding main processor is currently asserting its internal error signal and a second bit of each pair is indicative of whether the corresponding main processor has asserted its internal error signal previously.

4 (original). The system of claim 1, wherein the error logic is functional substantially immediately following the application of power to the data processing system.

5 (original). The system of claim 1, wherein the error logic includes an error detection unit configured to receive an internal error signal from each of the main processors and further configured to generate an error detect signal responsive to assertion of an internal error signal by any of the processors.

6 (original). The system of claim 5, wherein the error logic further includes error logging logic configured to receive the error detect signal and, responsive thereto, to update an error status register to reflect the internal error signal.

7-8 (canceled).

9 (currently amended). The system of claim ~~[8]~~ 1, wherein responsive to the service processor interrupt, the service processor is configured to ~~[powering]~~ power down the system.

10 (currently amended). Error detection logic suitable for use in a data processing system having multiple main processors, wherein the error detection logic is external to the main processors and is configured to receive internal error signals asserted by ~~[one or more]~~ the main processors ~~[of the data processing system]~~ and further configured to respond to an internal error signal by disabling ~~[the]~~ a processor asserting the ~~[signal and restarting]~~ signal, generating a service processor interrupt, and restarting the system with any remaining functional processors and further wherein the error detection logic includes an error status register externally accessible via an I2C bus.

11 (currently amended). The error logic of claim 10, wherein the error logic is further configured to record the internal error signal in ~~[an]~~ the error status register of the error logic.

12 (original). The error logic of claim 11, wherein the error status register includes at least a pair of bits corresponding to each of the main processors, wherein a first bit of each pair is indicative of whether the corresponding main processor is currently asserting its internal error signal and a second bit of each pair is indicative of whether the corresponding main processor has asserted its internal error signal previously.

13 (original). The error logic of claim 10, wherein the error logic is functional substantially immediately following the application of power to the data processing system.

14 (original). The error logic of claim 10, wherein the error logic includes an error detection unit configured to receive an internal error signal from each of the main processors and further configured to generate an error detect signal responsive to assertion of an internal error signal by any of the processors.

15 (currently amended). The error logic of claim 14, wherein the error logic further includes error logging logic configured to receive the error detect signal and, responsive thereto, to update ~~[an]~~ the error status register to reflect the internal error signal.

16 (currently amended). The error logic of claim 15, wherein the error logic is further configured to generate ~~[a]~~ the service processor interrupt responsive to error status register update.

17-20 (canceled).